1. A method for fabricating an array of capacitors for dynamic random access memory (DRAM) devices comprising the steps of:

providing a substrate having partially completed device areas for said DRAM devices;

forming a first insulating layer over said substrate;

forming first openings in said first insulating layer and forming capacitor node contact plugs in said first openings to said substrate;

depositing a second insulating layer and forming second openings for capacitor bottom electrodes aligned over and to said node contact plugs;

forming a first conducting layer in said second openings to form said capacitor bottom electrodes;

patterning said second insulating layer to leave portions between and contacting adjacent said bottom electrodes to provide physical support for said bottom electrodes, and to expose portions of outer sidewalls of said bottom electrodes for increased capacitance;

forming an interelectrode dielectric layer on said bottom electrodes, and depositing and patterning a second conducting layer to form top electrodes for said array of capacitors.

2. The method of claim 1, wherein said first insulating layer is silicon oxide deposited by chemical vapor

deposition, and is deposited to a thickness of between about 100 and 5000 Angstroms.

3. The method of claim 1, wherein said capacitor node contact plugs are formed from an electrically conducting material selected from the group that includes doped polysilicon, tungsten, aluminum-copper, and copper.

4. The method of claim 1, wherein said second insulating layer is silicon oxide deposited by chemical vapor deposition.

5. The method of claim 1, wherein said second insulating layer is deposited to a thickness of between about 1000 and 100000 Angstroms.

6. The method of claim 1, wherein said first conducting layer is an electrically conducting material selected from the group that includes doped polysilicon, metal silicide, copper, aluminum, and tungsten.

7. The method of claim 1, wherein said interelectrode dielectric layer is a material selected from the group that includes silicon oxide/silicon nitride/silicon oxide and tantalum pentoxide.

8. The method of claim 1, wherein said interelectrode dielectric layer is a high k dielectric.

9. The method of claim 8, wherein said high k dielectric material is a metal oxide, a metal nitride, a metal silicate, a transition-metal oxide, a transition-metal nitride, a transition-metal silicate, an oxynitride of a metal, a metal aluminate, zirconium silicate, zirconium aluminate, HfO_2, ZrO_2, ZrO_xN_y, HfO_xN_y, $HfSi_xO_y$, $ZrSi_xO_y$, $HfSi_xO_yN_z$, $ZrSi_xO_yN_z$, Al_2O_3, TiO_2, Ta_2O_5, La_2O_3, CeO_2, $Bi_4Si_2O_{12}$, WO_3, Y_2O_3, $LaAlO_3$, $Ba_{1-x}Sr_xTiO_3$, PbTiO3, $BaTiO_3$, $SrTiO_3$, $PbZrO_3$, PST, PZN, PXT, PMN, or a combination thereof.

10. The method of claim 1, wherein said second conducting layer is an electrically conducting material selected from the group that includes doped polysilicon, copper and aluminum.

11. A method for fabricating an array of capacitors for dynamic random access memory (DRAM) devices comprising the steps of:

providing a substrate having partially completed device areas for said DRAM devices;

forming a first insulating layer composed of silicon oxide on said substrate;

forming first openings in said first insulating layer

and forming capacitor node contact plugs in said first openings to said substrate;

depositing a second insulating layer and forming second openings for capacitor bottom electrodes aligned over and to said node contact plugs;

depositing a first conducting layer and polishing back to form said capacitor bottom electrodes in said second openings;

patterning said second insulating layer to leave portions between and contacting adjacent said bottom electrodes to provide physical support for said bottom electrodes, and to expose portions of outer sidewalls of said bottom electrodes for increased capacitance;

forming an interelectrode dielectric layer on said bottom electrodes, and depositing and patterning a second conducting layer to form top electrodes for said array of capacitors.

12. The method of claim 11, wherein said first insulating layer composed of silicon oxide is deposited by chemical vapor deposition, and is formed to a thickness of between about 1000 and 5000 Angstroms.

13. The method of claim 11, wherein said capacitor node contact plugs are formed from an electrically conducting

material selected from the group that includes doped polysilicon, tungsten, aluminum-copper, and copper.

14. The method of claim 11, wherein said second insulating layer is silicon oxide deposited by chemical vapor deposition.

15. The method of claim 11, wherein said second insulating layer is deposited to a thickness of between about 1000 and 100000 Angstroms.

16. The method of claim 11, wherein said first conducting layer is an electrically conducting material selected from the group that includes doped polysilicon, metal silicide, copper, aluminum, and tungsten.

17. The method of claim 11, wherein said interelectrode dielectric layer is silicon oxide/silicon nitride/silicon oxide or tantalum pentoxide.

18. The method of claim 11, wherein said interelectrode dielectric layer is a high k dielectric.

19. The method of claim 18, wherein said high k dielectric material is a metal oxide, a metal nitride, a metal silicate, a transition-metal oxide, a transition-metal

nitride, a transition-metal silicate, an oxynitride of a metal, a metal aluminate, zirconium silicate, zirconium aluminate, HfO_2, ZrO_2, ZrO_xN_y, HfO_xN_y, $HfSi_xO_y$, $ZrSi_xO_y$, $HfSi_xO_yN_z$, $ZrSi_xO_yN_z$, Al_2O_3, TiO_2, Ta_2O_5, La_2O_3, CeO_2, $Bi_4Si_2O_{12}$, WO_3, Y_2O_3, $LaAlO_3$, $Ba_{1-x}Sr_xTiO_3$, PbTiO3, $BaTiO_3$, $SrTiO_3$, $PbZrO_3$, PST, PZN, PXT, PMN, or a combination thereof.

20. The method of claim 11, wherein said second conducting layer is an electrically conducting material selected from the group that includes doped polysilicon, copper and aluminum.

21. An array of capacitors for dynamic random access memory (DRAM) devices comprised of:

a substrate having partially completed device areas for said DRAM devices;

a first insulating layer having openings to said substrate;

capacitor node contact plugs in said first openings;

a second insulating layer with second openings aligned over and to said node contact plugs, and capacitor bottom electrodes in said second openings;

said second insulating layer having portions between and contacting adjacent said bottom electrodes, physically supporting said bottom electrodes, and portions of outer sidewalls of said bottom electrodes exposed for increased

capacitor area;

an interelectrode dielectric layer on said bottom electrodes, and capacitor top electrodes.

22. The structure of claim 21, wherein said first insulating layer has a thickness of between about 100 and 5000 Angstroms.

23. The structure of claim 21, wherein said capacitor node contact plugs are an electrically conducting material selected from the group that includes doped polysilicon, tungsten, aluminum-copper, and copper.

24. The structure of claim 21, wherein said second insulating layer has a thickness of between about 1000 and 100000 Angstroms.

25. The structure of claim 21, wherein said second insulating layer is silicon oxide.

26. The structure of claim 21, wherein said bottom electrodes are an electrically conducting material selected from the group that includes doped polysilicon, metal silicide, aluminum, copper, and tungsten.

27. The structure of claim 21, wherein said portions of

said second insulating layer connect each pair of said adjacent bottom electrodes.

28. The structure of claim 21, wherein said portions of said second insulating layer connect contiguously each four said adjacent bottom electrodes.

29. The structure of claim 21, wherein exposed portions of said outer sidewalls increase area of said bottom electrodes by at least 50 percent.

30. The structure of claim 21, wherein said interelectrode dielectric layer is silicon oxide/silicon nitride/silicon oxide or tantalum pentoxide.

31. The structure of claim 21, wherein said interelectrode dielectric layer is a high k dielectric.

32. The structure of claim 31, wherein said high k dielectric material is a metal oxide, a metal nitride, a metal silicate, a transition-metal oxide, a transition-metal nitride, a transition-metal silicate, an oxynitride of a metal, a metal aluminate, zirconium silicate, zirconium aluminate, HfO_2, ZrO_2, ZrO_xN_y, HfO_xN_y, $HfSi_xO_y$, $ZrSi_xO_y$, $HfSi_xO_yN_z$, $ZrSi_xO_yN_z$, Al_2O_3, TiO_2, Ta_2O_5, La_2O_3, CeO_2, $Bi_4Si_2O_{12}$, WO_3, Y_2O_3, $LaAlO_3$, $Ba_{1-x}Sr_xTiO_3$, PbTiO3, $BaTiO_3$,

$SrTiO_3$, $PbZrO_3$, PST, PZN, PXT, PMN, or a combination thereof.

33. The structure of claim 21, wherein said top electrodes are an electrically conducting material selected from the group that includes doped polysilicon, copper and aluminum.

34. The structure of claim 21, wherein said second insulating layer extends between pairs of said bottom electrodes.

35. The structure of claim 21, wherein said second insulating layer extends between four adjacent said bottom electrodes.